STATUS OF THE CLAIMS

Claims 1-31. (Canceled)

32. (Currently amended) A method of forming a capacitor in a semiconductor device, said method comprising:

forming a bottom conducting layer, wherein said bottom conducting layer forms a bottom electrode;

forming a dielectric layer over the bottom conducting layer;

forming a top conducting layer over the dielectric layer, wherein said top conducting layer forms a top electrode; and

annealing [[a]] <u>the</u> top conducting layer of the top electrode with an oxidizing gas anneal.

33. (Original) A method of forming a capacitor of claim 32, wherein said capacitor is formed over a conductive plug, said method further comprising depositing an oxygen barrier over said conductive plug prior to forming the bottom conducting layer.

34. (Original) A method of forming a capacitor of claim 32, said method further comprising: annealing the dielectric layer after it is formed.

35. (Original) A method of forming a capacitor of claim 32, wherein said bottom conducting layer is formed of a material selected from the noble metal group.

36. (Original) A method of forming a capacitor of claim 32, wherein said bottom conducting layer is formed of a metal.

37. (Original) A method of forming a capacitor of claim 32, wherein said bottom conducting layer is formed of a metal alloy.

38. (Original) A method of forming a capacitor of claim 32, wherein said bottom conducting layer is formed of a conducting metal oxide.

39. (Original) A method of forming a capacitor of claim 32, wherein said bottom conducting layer is formed of a metal nitride.

40. (Original) A method of forming a capacitor of claim 32, wherein said bottom conducting layer is formed of a material selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), Platinum Iridium (PtIr), Ruthenium, Ruthenium Oxide (RuO_2), Rhodium Oxide (RhO_2), Chromium Oxide (CrO_2), Molybdenum Oxide (MoO_2), Rhemium Oxide (ReO_3), Iridium Oxide (IrO_2), Titanium Oxides (TiO_1 or TiO_2), Vanadium Oxides (VO_1 or VO_2), Niobium Oxides (NbO_1 or NbO_2), and Tungsten Nitride (WNx, WN or W_2N).

41. (Original) A method of forming a capacitor of claim 40, wherein said bottom conducting layer is formed of a material selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), Platinum Iridium (PtIr), and Tungsten Nitride (WNx, WN or W_2N).

42. (Original) A method of forming a capacitor of claim 32, wherein said dielectric layer is a dielectric metal oxide layer.

43. (Original) A method of forming a capacitor of claim 32, wherein said dielectric layer has a dielectric constant between 7 and 300.

44. (Original) A method of forming a capacitor of claim 32, wherein said dielectric layer is formed of a material selected from the group consisting of: Tantalum Oxide, Tantalum Pentoxide (Ta_2O_5), Barium Strontium Titanate (BST), Aluminum Oxide ($A1_2O_3$), Zirconium Oxide (ZrO_2), Praseodymium Oxide (PrO_2), Tungsten Oxide (WO_3), Niobium Pentoxide (Nb_2O_5), Strontium Bismuth Tantalate (SBT), Hafnium Oxide (HfO_2), Hafnium Silicate, Lanthanum Oxide (La_2O_3), Yttrium Oxide (Y_2O_3), and Zirconium Silicate.

45. (Original) A method of forming a capacitor of claim 44, wherein said dielectric layer is formed of a material selected from the group consisting of: Tantalum Oxide, Tantalum Pentoxide (Ta_2O_5), Barium Strontium Titanate (BST), Strontium Bismuth Tantalate (BST), Aluminum Oxide ($A1_2O_3$), Zirconium Oxide (ZrO_2) and Hafnium Oxide (HfO_2).

46. (Original) A method of forming a capacitor of claim 45, wherein said dielectric layer is Tantalum Oxide and is crystalline or amorphous material.

47. (Currently amended) A method of forming a capacitor of claim [[46]] 45, wherein said dielectric layer is an amorphous dielectric layer which is heated to a temperature above 200 degrees Celsius to change said dielectric layer from an amorphous material to a crystalline material.

48. (Original) A method of forming a capacitor of claim 32, wherein said top conducting layer is formed of a material selected from the noble metal group.

49. (Original) A method of forming a capacitor of claim 32, wherein said top conducting layer is formed of a non-oxidizing metal permeable to oxygen.

50. (Original) A method of forming a capacitor of claim 32, wherein said top conducting layer is formed of a conducting metal oxide.

51. (Original) A method of forming a capacitor of claim 32, wherein said top conducting layer is formed of a material selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), Platinum Iridium (PtIr), Ruthenium, Ruthenium Oxide (RuO_2), Rhodium Oxide (RhO_2), Chromium Oxide (CrO_2), Molybdenum Oxide (MoO_2), Rhemium Oxide (ReO_3), Iridium Oxide (IrO_2), Titanium Oxides (TiO_1 or TiO_2), Vanadium Oxides (VO_1 or VO_2), and Niobium Oxides (NbO_1 or NbO_2).

52. (Original) A method of forming a capacitor of claim 51, wherein said top conducting layer is formed of a material selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), and Platinum Iridium (PtIr).

53. (Original) A method of forming a capacitor of claim 32, wherein said bottom and top conducting layers are formed of a material selected from the group consisting of: Platinum, Platinum Rhodium (PtRh), or Platinum Indium (PtIr) and said dielectric layer is a layer of Tantalum Oxide.

54. (Original) A method of forming a capacitor of claim 32, wherein said bottom and top conducting layers are formed of a material selected from the group consisting of: Platinum, Platinum Rhodium (PtRh), or Platinum Iridium (PtIr) and said dielectric layer is a layer of Barium Strontium Titanate (BST) or Strontium Bismuth Tantalate (SBT).

55. (Original) A method of forming a capacitor of claim 32, wherein said top conducting layers are formed of a material selected from the group consisting of: Platinum, Platinum Rhodium (PtRh), or Platinum Iridium (PtIr) and said bottom conducting layer is a layer of Tungsten Nitride (WN_x, WN or W_2N) layer and said dielectric layer is a layer of Aluminum Oxide ($A1_2O_3$).

56. (Canceled).

57. (Original) A method of forming a capacitor of claim 56, wherein said annealing is performed with a material selected from the group consisting of: Oxygen (O_2), Ozone (O_3), Nitrous Oxide (N_2O), Nitric Oxide (NO), and water vapor (H_2O).

58. (Original) A method of forming a capacitor of claim 57, wherein said annealing is performed with a gas mixture containing at least one element selected from the group consisting: Oxygen (O_2), Ozone (O_3), Nitrous Oxide (N_2O), Nitric Oxide (NO), and water vapor (H_20).

59. (Original) A method of forming a capacitor of claim 56, wherein said annealing is a plasma enhanced annealing.

60. (Original) A method of forming a capacitor of claim 59, wherein said annealing is a remote plasma enhanced annealing.

61. (Original) A method of forming a capacitor of claim 56, wherein said annealing is an ultraviolet light enhanced annealing.

62. (Original) A method of forming a capacitor of claim 32, wherein said annealing is performed at a temperature between 300 and 800 degrees Celsius.

63. (Original) A method of forming a capacitor of claim 62, wherein said annealing is performed at a temperature between 400 and 750 degrees Celsius.

64. (Original) A method of forming a capacitor of claim 32, wherein said annealing is performed at a pressure between 1 and 760 torr.

65. (Original) A method of forming a capacitor of claim 64, wherein said annealing is performed at a pressure between 2 and 660 torr.

66. (Original) A method of forming a capacitor of claim 32, wherein said annealing is performed for between 10 seconds and 60 minutes.

67. (Original) A method of forming a capacitor of claim 66, wherein said annealing is performed for between 10 seconds and 30 minutes.

68. (Original) A method of forming a capacitor of claim 32, wherein said annealing is performed in the presence of an oxygen as with a gas flow rate between 0.01 and 10 liters per second.

Claims 69-96. (Canceled)

97. (Previously presented) A method of forming a capacitor in a semiconductor device, said method comprising:

forming a bottom conducting layer, wherein said bottom conducting layer forms a bottom electrode;

forming a dielectric layer over the bottom conducting layer;

forming a top electrode over said dielectric layer, said top electrode comprising at least one top conducting layer; and

annealing said at least one top conducting layer of said top electrode with an oxidizing gas anneal.